PTO
jc033 U.S.
09/808140
03/19/01

| Subclass | ISSUE CLASSIFICATION |
|---|---|
| Class | |

PATENT NUMBER

# U.S. UTILITY Patent Application

| O.I.P.E. | PATENT DATE |
|---|---|
| SCANNED ____ Q.A. ____ | |

| APPLICATION NO. | CONT/PRIOR | CLASS | SUBCLASS | ART UNIT | EXAMINER |
|---|---|---|---|---|---|
| 09/808140 | | 324 | 522 | 2858 | Deb |

APPLICANTS: William Corr

TITLE: Circuit for measuring on-chip power supply integrity

PTO-2040
12/99

## ISSUING CLASSIFICATION

| ORIGINAL | | CROSS REFERENCE(S) | |
|---|---|---|---|
| CLASS | SUBCLASS | CLASS | SUBCLASS (ONE SUBCLASS PER BLOCK) |
| | | | |
| INTERNATIONAL CLASSIFICATION | | | |
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☐ Continued on Issue Slip Inside File Jacket

| ☐ TERMINAL DISCLAIMER | DRAWINGS | | | CLAIMS ALLOWED | |
|---|---|---|---|---|---|
| | Sheets Drwg. | Figs. Drwg. | Print Fig. | Total Claims | Print Claim for O.G. |
| | | 1 | | | |

☐ The term of this patent subsequent to _____ (date) has been disclaimed.

_____ (Assistant Examiner) _____ (Date)

NOTICE OF ALLOWANCE MAILED

☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____

_____ (Primary Examiner) _____ (Date)

ISSUE FEE

| Amount Due | Date Paid |
|---|---|
| | |

☐ The terminal ___ months of this patent have been disclaimed.

_____ (Legal Instruments Examiner) _____ (Date)

ISSUE BATCH NUMBER

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